N-TYPE SILICON ELECTRON MOBILITY AND ITS RELATIONSHIP TO THE KINK EFFECT FOR NANO-SCALED SOI NMOS DEVICES

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Abstract. Electron mobility for the silicon-based devices is one of the most important parameters, which determine behavior of the components. Mobility depends on the silicon purity, doping level, presence of the lattice defects and electric field in the particular device. This influences are particularly important for the nano-scaled devices since it is much more difficult to control the thickness of the active layer, uniformity of impurity doping and appearance of parasitic bipolar devices and capacitances. We have investigated a relationship between electron mobility for the silicon based PD (Partially Depleted) SOI (Silicon On Insulator) NMOS (n-type Metal Oxide Semiconductor) Devices, and related kink effect which appears as a consequence of the charge accumulation at the interface of the Buried Oxide. We relate PD SOI NMOS Device technology parameters to the kink effect and we propose a guiding line for alleviating this effect.

Introduction

Silicon-on-insulator (SOI) CMOS offers a 20–35% performance gain over bulk CMOS [1]. As we move to the 0.1 μm generation and beyond, SOI is expected to be the technology of choice for system-on-a-chip applications which require high-performance CMOS, low-power, embedded memory, and bipolar devices [1]. The primary feature of MOS in SOI is that the local substrate ("body") of the device floats electrically, and therefore the substrate–source bias voltage, V_{BS}, is not fixed. This is especially prominent for Partially-Depleted (PD) SOI MOS devices where active layer is not totally depleted but it leaves an island of non-depleted region close to the buried oxide, Fig. 1. As V_{BS} changes, the device threshold voltage, V_T, will change. One manifestation of the threshold variation is the "kink effect," or increase in the output conductance of the device when drain-to-source bias, V_{DS}, comes near to 1 V, i.e. the band gap of silicon; however, the kink effect could appear even for the drain-to-source bias below the band gap of silicon, inset of the Fig. 1, [2]. This is caused by the impact-ionization induced increase in V_{BS} with increasing V_{DS}, and the resulting reduction of V_T; when V_{DS} becomes large enough, impact ionization current (holes) flows to the non-depleted body, increasing the body charge and V_{BS}, resulting in a decrease in V_T. This is much more pronounced for SOI NMOS devices than for SOI PMOS devices because effective cross-section for impact ionization is much higher for electrons than for holes. For this reason we will restrict our consideration to NMOS devices although the same approach could be implemented for PMOS.

Theory

Numerical modeling of the kink effect was already reported [3, 4]. However, there is a single article, to our knowledge, published so far, that deals with purely analytical modeling of the kink effect [5]. Although they take very profound physical properties into consideration, derived mathematical expressions are cumbersome and difficult for practical implementation. In this article

we show that it is possible to make an analytical model of the kink effect for PD SOI NMOS devices with the channel length below 600 nm based on electron drift properties in the channel. We directly relate kink effect and effective electron mobility in the channel, and thus we obtain quite feasible formula. We fit previously published experimental data for the kink to our theory introducing a single fitting parameter and from that point forward we predict behavior of the kink for various technology parameters for PD SOI NMOS. This theory is applicable for devices with effective gate length below 600 nm.

In this consideration we will employ classical mechanics. The first question arises: could we properly model electron drift in the channel by classical mechanics? At the Fig. 2 we give electron velocity in the channel vs. distance as calculated by classical mechanics and Monte-Carlo method [6]. As can be seen, Fig. 2, there is apparent difference between these two approaches for electron velocity along the channel, but maximum velocity is the same in both cases. What matters to us in estimating the kink effect is maximum electron velocity that the electron has at the drain interface.

At the Fig. 3 we give electron velocity vs. distance along the channel, as calculated by classical mechanics, for different channel lengths and for the same drain-to-source bias $V_{DS} = 1$V. Velocity is derived from differential equation for electron drift:

$$mv\frac{dv}{dx} = q\frac{V_{DS}}{L} - \frac{q}{\mu}v \tag{1}$$

where m is the electron rest mass, x is the distance along the channel, v is the electron drift velocity along the channel, q is the electron charge, V_{DS} is the drain-to-source bias, L is the channel length and μ is the electron mobility in the channel. Solution to this differential equation is:

$$v = \frac{\mu V_{DS}}{L}\left(1 + ProductLog\left(-e^{-1-\frac{qL}{m\mu^2 V_{DS}}x}\right)\right) \tag{2}$$

where *ProductLog*[z] gives the principal solution for w in $z = we^w$.

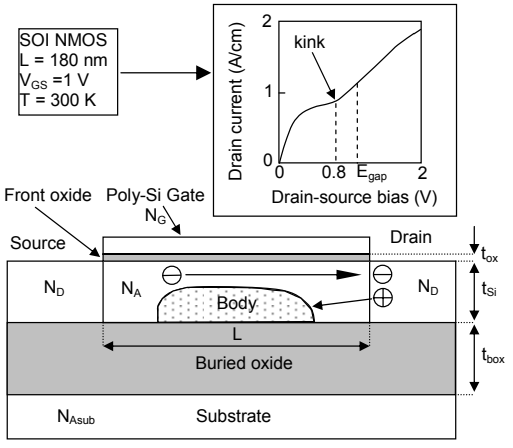

Fig. 1. Schematic representation of the Partially Depleted SOI NMOS device. Mechanism of impact ionization and kink is sketched. At the inset, typical drain current characteristic is shown [2].

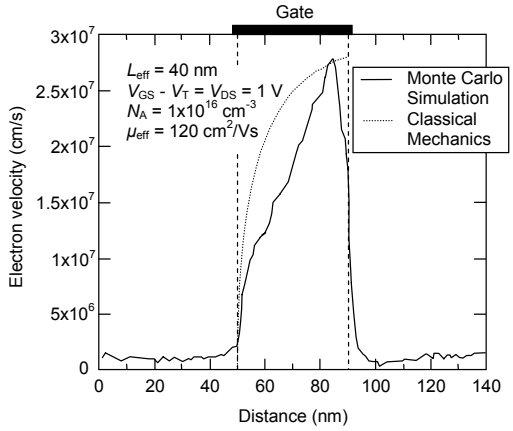

Fig. 2. Electron velocity vs. distance in the channel. Comparison between Monte Carlo simulation [6] and Classical Mechanics. $L_{eff} = 40$ nm, $V_{GS} - V_T = V_{DS} = 1$ V, $N_A = 1\text{x}10^{16}$ cm^{-3}, estimated effective mobility $\mu_{eff} = 120$ cm^2/Vs.

As can be seen on Fig. 3 there are two distinct regions of electron drift. First region belongs to the acceleration, where electron is accelerated up to the saturation velocity $v_{sat} = \mu V_{DS}/L$, and after that region it travels with constant velocity v_{sat}. On the Fig. 3 it is shown that for sufficiently short channel, electron will not attain saturation velocity at the point where it reach drain interface; this is pointed out by two different curves that depict extrapolated saturation velocity and terminating velocity at the drain interface. For channel lengths below 600 nm, we need to extrapolate electron drift in order to find saturation velocity. Below 600 nm there is apparent difference between terminating velocity and extrapolated saturation velocity, Fig. 3. Key assumption to us is that the electron will suffer no recombination in the acceleration region. In that manner, the same electrons that emerge at the source will immerge at the drain; this means that we are able to model situation at the drain interface knowing situation at the source. This assumption is reminiscent of the famous Shockley theory of the "lucky electron" where "lucky electron" will travel all the way through the channel without collisions with phonons, or it could even receive more phonons than it emits, so final velocity will be above the average. Here we only expect the electron not to suffer recombination during flight; but we consider no ballistic electrons.

Taking all this into account we will restrict our theory only to the electrons where extrapolated saturation velocity and terminating velocity do not equal. Now we have a possibility to formulate our basic model. Impact ionization in the drain region will occur if saturation energy is equal to the silicon band-gap energy:

$$E_{gap} = \frac{1}{2} m v_{sat}^2 = \frac{1}{2} m \left(\frac{\mu V_{kink}}{L} \right)^2 \tag{3}$$

where V_{kink} is the drain-to-source bias at the onset of the kink effect. This comes from the observation that all electrons emerging from the source, no matter what initial velocity they have, are accelerated towards saturation velocity v_{sat}. It is straightforward from here to express the kink voltage:

$$V_{kink} = \frac{L}{\mu} \sqrt{\frac{2E_{gap}}{m}} \tag{4}$$

Very special issue in this approach is modeling of the electron mobility in the channel. There

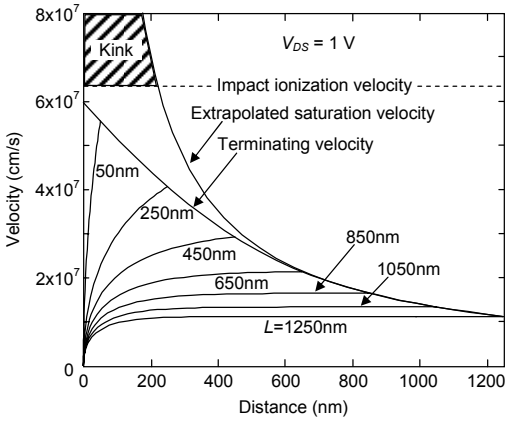

Fig. 3. Velocity in the channel vs. distance for different channel lenghts. Terminating velocity at the drain interface and extrapolated saturation velocity are also depicted. Shaded area represents the onset of the kink. Drain-to-soure bias is 1V.

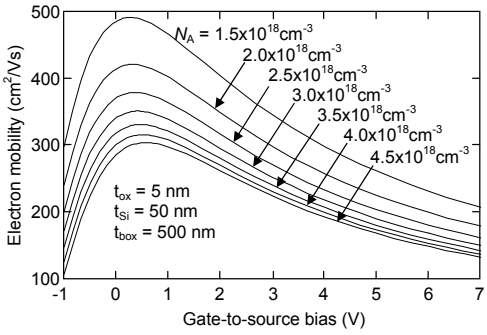

Fig. 5. Electron mobility in the channel vs. gate-to-source bias for different doping concentrations.

is no universal model that depends on geometry and technology parameters of SOI device. In this situation we will employ two successive stages in mobility modeling. First, we will find mobility for the doped Si with the same doping that active layer is made of. We use semi-empirical formula [9]:

$$\mu = 200\frac{cm^2}{Vs}\left(1+\frac{2\times10^{18}cm^{-3}}{N_A}\right) \tag{5}$$

where μ is the electron mobility of silicon depending only on doping concentration. This value will be used as maximum mobility in the channel of the SOI NMOS. In the second stage of the mobility modeling we will introduce this expression:

$$\mu_{eff} = \frac{2\sqrt{b}\mu\left(E_s+\sqrt{b}\right)}{b+\left(E_s+\sqrt{b}\right)^2} \tag{6}$$

where μ_{eff} is the effective electron mobility in the channel, E_s is the transverse electric field in the front channel, V_{GS} is the gate-to-source bias, V_T is the threshold voltage, μ is the maximum mobility as calculated from (5), and b is the fitting parameter. E_s depends on the gate-to-source bias. In (6) it is envisioned that maximum mobility corresponds to the threshold bias V_T according to the experimental results in [10]. Therefore, we need to find the threshold for a given device technology. We use kvazi 2 D formula obtained through full depletion approximation [11]. Threshold formula read as [11]:

$$\begin{aligned} V_T = {} & V_{FB} - 2\phi_f + \frac{t_{ox}}{t_{box}+\gamma t_{Si}}\left(-2\phi_f - V_{BS} + V_{FBsub} + \frac{qN_A t_{Si}\left(2t_{box}+\gamma t_{Si}\right)}{2\gamma\varepsilon_{Si}}\right) \\ & - \frac{t_{box}+\gamma t_{Si}}{t_{box}+t_{ox}+\gamma t_{Si}}\frac{\left[2(V_{BI}-2\phi_f)+V_{DS}\right]}{2ch(L_G/2\lambda)-2} \end{aligned} \tag{7}$$

where V_{FB} is the flat-band voltage in the front channel, q is the electron charge, ϕ_f is the Fermi level, $\gamma=\varepsilon_{Si}/\varepsilon_{ox}$ is a dimensionless constant, ε_{Si} is the dielectric permittivity of silicon, ε_{ox} is the dielectric permittivity of SiO_2, V_{FBsub} is the flat-band voltage in the back channel, V_{BS} is the substrate-to-source bias.

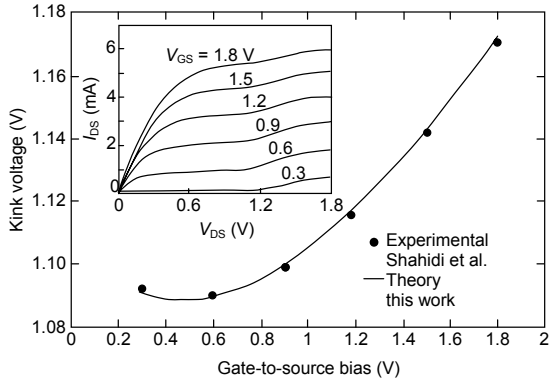

Fig. 5. Kink voltage vs. gate-to-source bias. Comparison with experimental data from Shahidi et al. [12]. As the inset we give original drain-to source current characteristics from which kink data is derived [12].

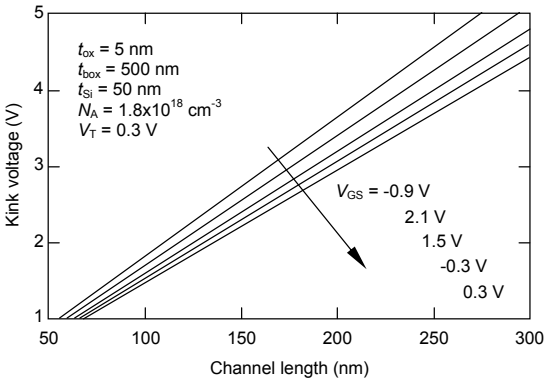

Fig. 6. Kink voltage vs. channel length depending on the gate-to-source bias.

Results and discussion

Fig. 4 depicts electron mobility in the channel vs. gate-to-source bias as calculated by (6) for different doping concentrations. Mobility is lowered in the whole range of V_{GS} as active layer doping is increased. Maximum mobility corresponds to the threshold bias voltage. This mobility model enables us to predict the onset of the kink effect.

To validate this model we will compare it to the experimental results. Fig. 5 shows kink voltage vs. gate bias for the device with technology parameters: t_{ox} = 4 nm, t_{Si} = 126 nm, t_{box} = 360 nm, $N_A = 2x10^{18}cm^{-3}$, [12]. On the Fig. 5 we compare experimental results from Shahidi et al. [12] and theoretical results from this work for SOI NMOS device. As the inset of the Fig. 5 we give original drain current characteristic from which kink data is derived [12]. Theoretical curve is fitted to the experimental data through a single fitting parameter *b* in (6). By this fitting we directly relate electron mobility in the channel and the corresponding kink voltage. The kink voltage is the lowest at the threshold, Fig. 5, reflecting the fact that electron mobility has maximum at the threshold, Fig. 4, [10]. From this point forward we predict behavior of the kink effect for various technology parameters for PD SOI NMOS devices, Fig. 6. At Fig. 6 we give prediction for the kink voltage vs. channel length for the different gate-to-source bias. The threshold voltage for this component is V_T = 0.3 V. As can be seen at the Fig. 6, the kink voltage exhibits linear behavior depending on the gate length. Lowest slope is for the gate-to-source bias equaling to the threshold voltage. Moving below or above threshold will increase the slope for the kink voltage dependence on channel length, Fig. 6. Increase in doping concentration renders increase in the kink voltage in the whole range of the gate-to-source bias, due to decrease in electron mobility, Fig. 7(a). Variations in the active layer thickness will bring small changes in the kink voltage for the gate-to-source bias near threshold, Fig. 7(b), but it will bring remarkable decrease in the kink voltage with increasing active layer thickness as we move eider below or above threshold. Increasing front oxide thickness will increase kink voltage in the region below threshold, but it will decrease kink voltage in the region above threshold, Fig. 7(c). However, kink voltage change due to the variations in the front oxide thickness

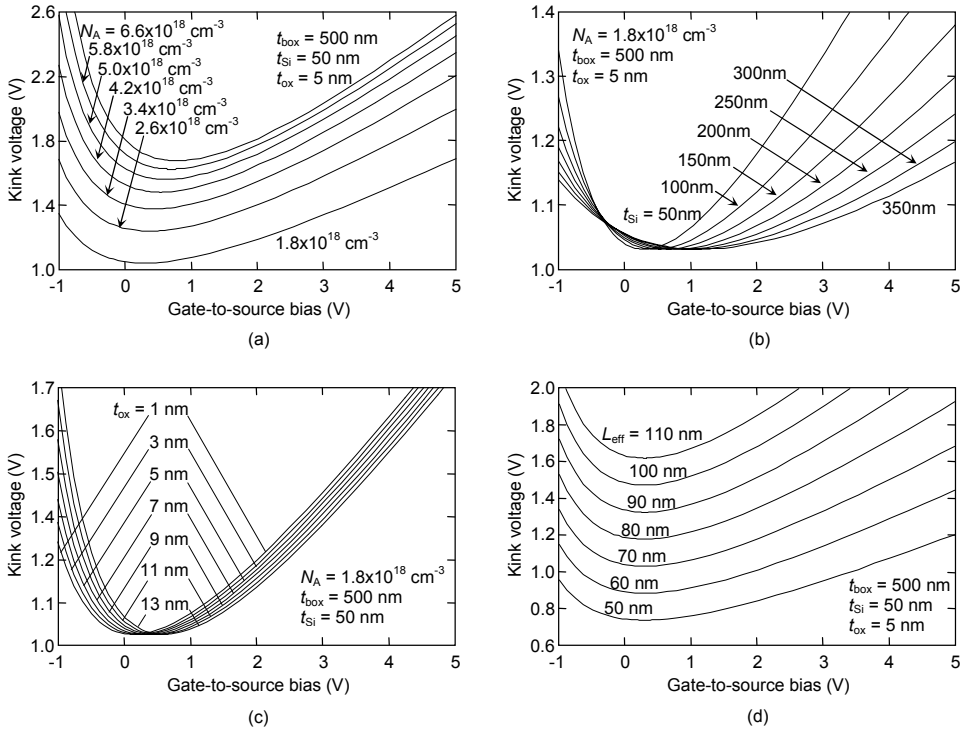

Fig. 7. Kink voltage vs. gate-to-source bias depending on (a) active layer doping concentration, (b) thickness of the active layer, (c) front oxide thickness, (d) channel length.

is not so prominent. Decrease in the channel length will decrease kink voltage in the whole range of the gate-to-source bias thus making device more prone to the kink, Fig. 7(d).

In designing PD SOI NMOS devices, in order to avoid the kink effect, according to this work we need to follow these rules: channel doping should be high thus increasing the kink voltage and allowing component more broad range of safe operation, Fig. 7(a). Active layer should be thin as much as possible because that will significantly increase the kink voltage and render component more resistible to the kink, Fig. 7(b). Front oxide thickness is particular trade-off since decrease in its thickness will decrease the kink voltage when component is operating below threshold thus increasing leakage current in the off-state, but the same decrease in the front oxide thickness will increase the kink voltage when component is operating above threshold thus making device more stable in the saturation regime, Fig. 7(c).

Conclusion

We have shown that it is possible to directly relate electron mobility in the channel for PD SOI NMOS devices to the kink voltage i.e. triggering drain-to-source bias at the onset of the kink effect. This approach could be used in two manners: first, to give prediction for behavior of the kink voltage for various technology parameters; this can be utilized in modeling of PD SOI NMOS devices or circuitry simulations; second, it could be new method for measuring electron mobility in the front channel of these devices, i.e. knowing kink voltage we are able to derive corresponding electron mobility. It is important to notice that theory is applicable for the devices with channel lengths below 600 nm.

References

[1] G. G. Shahidi, "SOI technology for the GHz era", *IBM J. RES. & DEV.* VOL. 46, NO. 2/3 MARCH/MAY 2002.

[2] Shahidi, et al. IBM DAMOCLES tutorial. Available at: www.research.ibm.com/DAMOCLES/html_file/segii.html

[3] H. K. Yu, J. S. Lyu, S. W. Kang and C. K. Kim, "A physical model of floating body thin film silicon-on-insulator nMOSFET with parasitic bipolar transistor", *IEEE Trans. Electron Devices* 41, 726 (1994).

[4] D. Suh and J. G. Fossum, " A physical charge-based model for non-fully depleted SOI MOSFET's and its use in assessing floating-body effects in SOI CMOS circuits", *IEEE Trans. Electron Devices* 42, 728 (1995).

[5] S. S. CHEN and J. B. KUO, "An Analytical CAD Kink Effect Model of Partially-Depleted SOI NMOS Devices Operating in Strong Inversion", *Solid-State Electronics*, Vol. 41. No. 3, pp. 447-458, 1997.

[6] S. Barraud, L. Clavelier, T. Ernst, "Electron transport in thin SOI, strained-SOI and GeOI MOSFET by Monte Carlo simulation", *Solid State Electronics*, 49 (2005) 1090-1097.

[7] Jacoboni C, Nava F, Canali C, Ottaviani, "Electron drift velocity and diffusivity in germanium", G, *Phys Rev B*, 1981, 24, 1014-26.

[8] S. Takagi and A. Toriumi, “New Experimental Findings on Hot Carrier Transport under Velocity Saturation Regime in Si MOSFETs,” *IEDMDig.*, 7 1 l-7 14 (1992).

[9] Siegfried Selberherr, *Analysis and Simulation of Semiconductor Devices*, pp. 88, Wien, Springer-Verlag, 1984.

[10] J. R. Davis, A. E. Glaccum, K. Reeson, and P. L. F. Hemment, “Improved Subthreshold Characteristics of n-Channel SOI Transistors,” *IEEE Elec. Dev. Let.*,7(10), 570-572 (1986).

[11] Milija Sarajlić, Rifat Ramović, "Modification of the Quasi 2D Model for Short-Channel SOI MOSFET", *Proc. ETRAN,* Budva, Serbia and Montenegro, June , 2005.

[12] G. G. Shahidi, J. D. Warnock, J. Comfort, S. Fischer, P. A. McFarland, A. Acovic, T. L. Chappell, B. A. Chappell, T. H. Ning, C. J. Anderson, R. H. Dennard, J. Y.-C. Sun, M. R. Polcari, B. Davari, " CMOS scaling in the 0.1 ㎜, 1 .X-volt regime for high-performance applications", *IBM J. RES. & DEV.* VOL. 39, NO. 1/2, JANUARY/MART 1995.